UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,880	03/03/2004	Satoru Akiyama	500.4358IX00	4729

20457 7590 12/16/2008

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
12/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,880	AKIYAMA ET AL.	
	Examiner	Art Unit	
	Denise Tran	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-12 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-12 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/6/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/10/08 has been entered.

2. The applicant's amendment filed 11/10/08 has been considered. Claims 1-3, 6-12, and claims 20-28 are presented for examination. Claims 4-5 and 13-19 have been canceled.

3. In response to the Applicant STATEMENT OF SUBSTANCE OF INTERVIEW , during the telephone interview conducted on November 7, 2008, the examiner did not state or "advised the undersigned attorney that it would be required to file an RCE to obtain full consideration of the November 5, 2008 Amendment."

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim(s)_1-12 of patent 7,301791_ contain(s) every element of claim(s)_ 1-3 of the instant application and as such anticipate(s) claim(s)_ 1-3 of the instant application.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-3, 6-12, and 20-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

claim 1, it's unclear whether "said write operation" directed to "a write operation" on line 3 or a write operation to the cache or a write operation back to a memory. Claims 2-3, 6-12, and 20-28 have similar problems as discussed in claim 1.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 6-12 and 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al., US 2003/0033492, (hereinafter Akiyama), in view of Atwood et al., "SESO Memory: a CMOS Compatible High Density Embedded Memory technology for Mobile Applications, " 2002, Symposium on VLSI Circuit Digest of Technical Papers pp. 154-155, (2000) (hereinafter Atwood).

Claim 1, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

wherein, when first data is written into said semiconductor device from the outside, and when said cache memory does not hold an address at which said first data is to be written (e.g., [0056]), data held in an associated entry of said cache memory is written back to one of said plurality of memory banks (e.g., [0056]), and said first data is written into said cache memory (e.g., [0056]), and

wherein, when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank included in said plurality of memory banks (i.e., data is written to only the selected bank and the other banks cannot access or are idle from the write operation, e.g., [0058]; [0059]; [0061]; [0067]).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

Claim 20, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

an internal data bus for coupling said cache memory to said memory banks (e.g., page 11, claim 5); and

a plurality of data input/output nodes for inputting/outputting data from/to the outside (e.g., page 11, claim 5),

wherein said cache memory has a cache line comprised of a plurality of sublines (e.g., page 11, claims 1 and 5), and

A=N.B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus (e.g., page 11, claim 5),

Wherein, when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks (i.e., data is written to only the selected bank and the other banks cannot access or are idle from the write operation, e.g., [0058]; [0059]; [0061]; [0067]).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

Claims 2-3, and 21-22, Akiyama teaches said cache memory has a plurality of sets corresponding to the number of ways, and each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks (e.g., [0090]); when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory (e.g.,[0030]).

Claims 6-7 and 23, Akiyama teaches a plurality of data input/output nodes for inputting/outputting data to/from the outside, wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device; an internal data bus for coupling said cache memory to said memory banks (e.g., page 11, claim 5; page 3, [0027]); wherein said cache memory has a cache line comprised of a plurality of sublines, and A=N. B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus (e.g., page 11, claim 5); said cache memory has a plurality of flags each associated with one subline for managing data held thereon (e.g., fig. 3A, v0-v3, D0-D3);

Claims 8-9, 12, 24-25, and 28, Akiyama teaches when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank (e.g., fig. 2B, S205; [0057]-[0058]); when a flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory (e.g., [0058]); and wherein said cache memory comprises SRAM memory cells [e.g., 0027].

Claims 10-11 and 26-27, Akiyama teaches wherein said cache memory comprises SRAM memory cells [0027]. Akiyama does not explicitly show wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or a phase change memory cell. Atwood teaches memory cell is either a SESO (Single Electron Shut Off) memory cell or a phase change memory cell (e.g., page 154, column 2, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

10. Applicant's arguments filed 11/10/08 have been fully considered but they are not persuasive.

11. In the remarks, the applicant argued that there is no teaching of writing data back to a second memory bank, different from the first memory bank, when the first memory bank cannot accept access from the outside. Further, it is respectfully submitted that there is absolutely nothing that Akiyama teaches that would lead one to write data back to a second memory bank, rather than a first memory bank, when the reason that the first memory bank cannot accept the access from the outside is due to a write operation.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., write data back to a second memory bank, rather than a first memory bank) are not

recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Akiyama teaches what in the claims are : Claim 1, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

wherein, when first data is written into said semiconductor device from the outside, and when said cache memory does not hold an address at which said first data is to be written (e.g., [0056]), data held in an associated entry of said cache memory is written back to one of said plurality of memory banks (e.g., [0056]), and said first data is written into said cache memory (e.g., [0056]), and

wherein, when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank included in said plurality of

memory banks (i.e., data is written to only the selected bank and the other banks cannot access or are idle from the write operation, e.g., [0058]; [0059]; [0061]; [0067]).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, and paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

Claim 20, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

an internal data bus for coupling said cache memory to said memory banks (e.g., page 11, claim 5); and

a plurality of data input/output nodes for inputting/outputting data from/to the outside (e.g., page 11, claim 5),

wherein said cache memory has a cache line comprised of a plurality of sublines (e.g., page 11, claims 1 and 5), and

A=N.B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus (e.g., page 11, claim 5),

Wherein, when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside due to said write operation, the data is written back to a second memory bank, different from the first memory bank, included in said plurality of memory banks (i.e., data is written to only the selected bank and the other banks cannot access or are idle from the write operation, e.g., [0058]; [0059]; [0061]; [0067]).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, and paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

In further discussion, the examiner disagreed with the applicant argument. According to Akiyama teaches, for example [0058]; [0059]; [0061]; [0067], teaches writing data back to a second memory bank (bank 4), different from the first memory bank (one of the other banks), when the first memory bank cannot accept access from

the outside because they are not selected by a controller due to (an address controlling or enabling writing of) a write operation.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday and Thursday from 8:45 a.m. to 5:15 p.m.. The examiner can also be reached on alternate Friday

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung, can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Denise Tran/

Primary Examiner, Art Unit 2188